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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,124	08/25/2003	Aurelian Vasile Lazarut	X-1391 US	3211
24309	7590	11/02/2005	EXAMINER	
XILINX, INC ATTN: LEGAL DEPARTMENT 2100 LOGIC DR SAN JOSE, CA 95124			LEVIN, NAUM B	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/648,124

Applicant(s)

LAZARUT ET AL.

Examiner

Naum B. Levin

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

This office action is in response to application 10/648,124, and Amendment filed on 08/08/2005. Claims 1-30 remain pending in the application.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being unpatentable by Kittross et al. (US Patent 6,681,351).

2. As to claims 1, 6, 11, 16, 21 and 26 Kittross discloses:

(1) A client-server semiconductor verification system, said system comprising:  
a client device (user computer) storing a test job (test program 38/test procedures 40) for testing a design of a logic circuit, said test job having test vectors (test elements 42) and configuration data for programmable logic (instructions for configuring DUTs 46) (col.1, ll.11-26; col.4, ll. 32-46; col.7, ll.1-8; col.7, ll.31-36; col.13, ll.60-67; col.14, ll.1-2);

a server (processor) coupled to said client device, said server receiving said test job from said client device (col.4, ll. 48-58; col.14, ll.3-15); and

a system under test (devices under test/DUTs 46) coupled to said server and having programmable logic which is configured using said configuration data, said system under test receiving said test vectors and outputting result vectors to the client device by way of said server ("The arrows 30 of FIG. 1 represent information (i.e., signals) exchanged between the memory 22, the I/O device 24, the processor 26 and the test interface 28") (col.1, ll.48-58; col.6, ll.57-65; col.7, ll.20-30; col.12, ll.41-46);

(6) A client-server semiconductor verification system, said system comprising:

a plurality of client devices, wherein a client device of said plurality generates a test job for testing the design of a logic circuit and comprises test vectors and configuration data for programmable logic (col.1, ll.11-26; col.4, ll. 32-46; col.7, ll.1-8; col.7, ll.31-65; col.13, ll.60-67; col.14, ll.1-2);

a server coupled to said plurality of client devices by way of a network, said server receiving said test job from said client device (col.4, ll. 48-58; col.14, ll.3-15); and

a system under test coupled to said server, said system under test having programmable logic which is configured and receiving said test vectors and outputting result vectors to the client device by way of the server (col.1, ll.48-58; col.6, ll.57-65; col.7, ll.20-30; col.12, ll.41-46);

(11) A client-server semiconductor verification system, said system comprising:

a plurality of client devices, wherein a client device of said plurality generating a test job for testing the design of a logic circuit and having test vectors (col.1, ll.11-26; col.4, ll. 32-46; col.7, ll.1-8; col.7, ll.31-65; col.13, ll.60-67; col.14, ll.1-2);

a job distribution server coupled to said plurality of client devices by way of a network, said job distribution server receiving said test job from said client device (col.12, ll.25-39; col.13, ll.60-67; col.14, ll.1-2);

a server coupled to said plurality of client devices by way of said job distribution server, said server receiving said test job from said job distribution server (col.4, ll. 48-58; col.12, ll.41-46; col.14, ll.3-15); and

a system under test having programmable logic which is configured and being coupled to said server, said system under test receiving said test vectors and outputting result vectors to said client device by way of said server and said job distribution server (col.1, ll.48-58; col.6, ll.57-65; col.7, ll.20-30; col.12, ll.41-46);

(16) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

storing a test job for testing a design of a circuit in a client device, said test job having test vectors and configuration data for programmable logic (col.1, ll.11-26; col.4, ll. 32-46; col.7, ll.1-8; col.7, ll.31-36; col.13, ll.60-67; col.14, ll.1-2);

configuring a system under test having programmable logic by way of said test server (col.1, ll.11-26; col.4, ll. 32-46; col.7, ll.1-8; col.7, ll.31-36; col.13, ll.60-67; col.14, ll.1-2);

coupling said test vectors to said system under test (col.4, ll. 48-58; col.14, ll.3-15);

receiving an output comprising result vectors from said system under test (col.1, ll.48-58; col.6, ll.57-65; col.7, ll.20-30; col.12, ll.41-46); and

comparing said result vectors from said system under test to expected result vectors (col.1, ll.11-25);

(21) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client devices to a test server, each said client device storing a test job for testing the design of a logic circuit, said test job having test vectors and configuration data for programmable logic (col.1, ll.11-26; col.4, ll. 32-58; col.7, ll.1-8; col.7, ll.31-36; col.12, ll.41-46; col.13, ll.60-67; col.14, ll.1-15);

reconfiguring a system under test by way of said test server (col.1, ll.11-26; col.4, ll. 32-46; col.7, ll.1-8; col.7, ll.31-36; col.13, ll. 16-51; col.13, ll.60-67; col.14, ll.1-2);

coupling test vectors of a predetermined test job to said system under test by way of said test server (col.4, ll. 48-58; col.14, ll.3-15);

receiving an output comprising result vectors from said system under test (col.1, ll.48-58; col.6, ll.57-65; col.7, ll.20-30; col.12, ll.41-46); and

comparing said result vectors from said system under test to expected result vectors (col.1, ll.11-25);

(26) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client devices to a job distribution server, each said client device storing a test job for testing the design of a logic circuit and having test vectors and configuration data for programmable logic (col.1, ll.11-26; col.4, ll. 32-46; col.7, ll.1-8; col.7, ll.31-36; col.12, ll.25-39; col.13, ll.60-67; col.14, ll.1-2);

reconfiguring a system under test by way of said test server (col.1, ll.11-26; col.4, ll. 32-46; col.7, ll.1-8; col.7, ll.31-36; col.13, ll. 16-51; col.13, ll.60-67; col.14, ll.1-2);

coupling said job distribution server to a plurality of servers, each said server coupling predetermined test vectors to a system under test of a plurality of systems under test (col.1, ll.48-58; col.4, ll. 48-58; col.6, ll.57-65; col.7, ll.20-30; col.12, ll.25-46; col.13, ll.60-67; col.14, ll.1-15);

receiving an output comprising result vectors from a system under test of said plurality of systems under test (col.1, ll.48-58; col.6, ll.57-65; col.7, ll.20-30; col.12, ll.41-46); and

comparing said result vectors from said system under test to expected result vectors (col.1, ll.11-25).

3. As to claims 2-5, 7-10, 12-15, 17-20, 22-25 and 27-30 Kittross recites:

(2), (4), (18) The system/method, wherein said client device further has expected results (col.1, ll.11-25);

(3), (17) The system/method, wherein said client device generates said test vectors (col.7, ll.38-65);

(5)The system, wherein said test vectors and said expected results are generated by an external device (col.1, ll.26-43; col.7, ll.10-19);

(7), (23) The system of claim 6 wherein said server comprises a network interface (col.14, ll.3-15);

(8), (9), (14), (20), (24), (30) The system/method, wherein said server comprises a system under test interface (col.1, ll.48-58; col.6, ll.57-65; col.7, ll.20-30; col.12, ll.41-46);

(10), (19) The system/method further comprising another server coupled to said plurality of client devices by way of the network (col.13, ll.60-67; col.14, ll.1-15);

(12), (13), (15), (22), (27), (28), (29) The system/method further comprising a plurality of servers coupled to said plurality of client devices (col.4, ll. 48-58; col.12, ll.25-46; col.13, ll.60-67; col.14, ll.1-15);

(25) The method of claim 21 wherein said step of comparing comprises comparing said result vectors from said system under test to expected result vectors at said client device (col.1, ll.11-25).

### **Remarks**

4. Mostly Applicant argues "...there is no teaching or suggestion in Kittross of a client device and a server in a client-server semiconductor verification system."

Kittross describes, for example, automatic test equipment (ATE) system that includes the I/O device 24, the memory 22 and the processor 26, above components may form portions of a general purpose computer such as workstation or distributed computing system (col.13, lines 60-67; Fig.1). The term distributed computing system means that this system may include a client computer and server computer connected to each other by network like internet, ethernet or other remote connections.

So, distributed computing system in the reference corresponds to client-server system in the application, in more details, for example, I/O device in one of the



computers corresponds to the client and the processor in other computer corresponds to the server.

Kittross also, for example, recites: "The memory 22 may include ... other storage media (e.g., CDROM, network servers, etc.), or a combination different memory types. Additionally, the I/O device 24 may include multiple input and output devices such as one or more displays, keyboards, printers, mice, etc. (col.13, ll.63-67; col.14, ll.1-2; Fig.1)". In this passage memory 22 in the reference corresponds to the server/servers in the application, and input and output devices in the reference correspond to the client/clients in the application.

5. Next Applicant argues: the reference " does not include configuration data for programmable logic".

Kittross, for example, discloses: "...FIG. 6 shows, by way of example only, an instance editor window 100 which prompts the user to enter values for a particular instance of the test procedure 40. Accordingly, the user can develop the test program 38 so that it performs variations of the same test on the same device using multiple instances of the same test procedure 40 (col.11, ll.25-42)". In this passage variations using multiple instances to develop; the test program in the reference corresponds to configuration data for programmable logic in the application.

6. Applicant also argues: reference no teaching "job distribution server".

Kittross teaches, for example, "Alternatively, the processor 26 may have a multiprocessor configuration or a distributed processing configuration which controls the multiple processing units 27 respectively associated with the multiple devices 46.

(col.14, ll.7-10)". In this passage distributed processing configuration of the processor 26 corresponds to job distribution server in the application.

7. Examiner defined Applicant's arguments as none persuasive.

Accordingly **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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**VUTHE SIEK**  
**PRIMARY EXAMINER**